WHAT IS CLAIMED IS:

1. A digital system integrated on a semiconductor chip, comprising:

one or more first bus masters coupled to a first bus in a first clock domain;

a programmable logic device coupled to a second bus in a second clock domain;

a first bridge coupled between the first and second buses operable to de-couple the first clock domain from the second clock domain.

2. The system of claim 1, wherein one of the first bus masters comprises a central processing unit.

3. The system of claim 1, wherein the one or more first bus masters are configured to communicate with the one or more second bus slaves coupled to the second bus, via the first bridge.

4. The system of claim 1, wherein the programmable logic device comprises a second bus master.

5. The system of claim 4, further comprising a second bus bridge coupled between the second bus and the second bus master.

6. The system of claim 1, further comprising a plurality of second bus masters coupled to the second bus.

7. A digital system on a semiconductor chip, comprising:

a central processing unit (CPU)coupled to a first bus;

a programmable logic device (PLD) coupled to a second bus; and

a bus bridge coupled between the first and second buses.

8. The digital system of claim 7, wherein the first bus operates within a first clock domain and the second bus operates within a second clock domain.

9. The digital system of claim 8, wherein the first clock domain is characterized by a first clock frequency that is greater than a second clock frequency characteristic of the second clock domain.

8. The digital system of claim 7, wherein the first bus operates within a first clock domain and the second bus operates within a second clock domain.

9. The digital system of claim 8, wherein the first clock domain is characterized by a first clock frequency that is greater than a second clock frequency characteristic of the second clock domain.

10. The digital system of claim 8, wherein either or both of the first clock frequency and second clock frequency are programmable.

11. A digital system on a semiconductor chip, comprising:

a central processing unit (CPU) coupled to a first bus in a first clock domain defined by a first bus clock frequency;

a plurality of electronic devices coupled to a second bus in a second clock domain defined by a second bus clock frequency;

a bus bridge coupled between the first and second buses and operable to allow communication between the CPU at the first bus clock frequency and one of the plurality of electronic devices at the second bus clock frequency;

a programmable logic device (PLD) coupled to a third bus in a third clock domain; and

a PLD bridge coupled between the second and third buses.

12. A device comprising:

a first circuit operable in a first clock domain;

a first communication media coupled to the first circuit and configured to transfer information;

a second circuit operable in a second clock domain;

a second communication media coupled to the second circuit and the first communication media, wherein the second communication media configured to transfer information; and

a communication circuit coupled to the first and second communication medium and configured to provide communication between the first and second circuits.

13. The device of claim 12, wherein the device includes a plurality of circuits deposited on an integrated circuit.

14. The device of claim 12, wherein the first circuit is a processor.

15. The device of claim 12, wherein the first clock domain provides a first programmable clock frequency.

16. The device of claim 15, wherein the frequency of the first programmable clock frequency can be selectively programmed.

17. The device of claim 12, wherein the first communication media is a bus.

18. The device of claim 12, wherein the information includes data.

19. The device of claim 12, wherein the information includes control signals.

20. The device of claim 12, wherein the second circuit is a programmable logic device.

21. The device of claim 20, wherein the programmable logic device further includes:

a plurality of logic cells having at least one programmable circuit arranged in a multiple dimensional array; and

at least one interconnector coupled to the plurality of the logic cells and configured to transfer information between the plurality of the logic cells.

22. The device of claim 12, wherein the second clock domain includes a second programmable clock frequency.

23. The device of claim 22, wherein the first programmable clock frequency has the same frequency of the second programmable clock frequency.

24. The device of claim 12, wherein the communication circuit is a bus bridge.

25. The device of claim 24, wherein the bus bridge transfers the information between the first and second clock domains.